

REMARKS

This is in response to the Office Action mailed on November 3, 2004, and the references cited therewith.

Claims 1, 2, 5, 7, 10, 11, 15, 17, 18, 19, 27, 28, 34, 35, 41, 42, 45, 46, 49, 50, 53, and 54 are amended, no claims are canceled, and no claims are added; as a result, claims 1-69 are now pending in this application.

§102 Rejection of the Claims

Rejection of claims 1, 8, 10, 11, 18, 23, 27, 33, 34, 41, 45, 49, and 53:

Claims 1, 8, 10, 11, 18, 23, 27, 33, 34, 41, 45, 49, and 53 were rejected under 35 USC § 102(b) as being anticipated by Iwamoto et al. (U.S. Patent No. 6,292,040). Applicant has amended claims 1, 10, 18, 27, 34, 41, 45, 49, and 53, from which the remaining rejected claims depend, and respectfully traverses the rejection.

Iwamoto et al. disclose a circuit having a clock selector 20 (Figure 2) that is formed from a collection of subcircuits (e.g., NAND circuits, delay circuits, and inverter circuits). Selector 20 selectively outputs a clock signal, DIN, as either an external clock signal, EXTCLK, or an internal clock signal, INTCLK. Selector 20 is designed so that DIN is a multiple of EXTCLK. (See Figures 1, 2, and 3A-3H, and col. 8, line 8 through col. 9, line 21).

Applicant's claims 1, 18, 27, 34, 41, 45, 49, and 53, and the claims that depend therefrom, include at least the following features, which distinguish Applicant's claims from that which is disclosed by Iwamoto et al.:

“... a signal selector circuit to switch between providing an external clock signal or a feedback clock signal as an input clock signal to a delay line based on a detected jitter between the external clock signal and the feedback clock signal . . .”

Applicant's claim 10 and the claims that depend therefrom, include at least the following features, which distinguish Applicant's claims from that which is disclosed by Iwamoto et al.:

“ . . . a signal selector circuit, coupled to the delay line and the feedback loop to switch between a delay locked loop mode and a phase locked loop mode based on a detected jitter between the external clock signal and the feedback clock signal, wherein in the delay locked loop mode, the signal selector circuit is to provide an external clock signal as the input clock signal to the delay line, and in the phase locked loop mode, the signal selector circuit is to provide the feedback clock signal as the input clock signal to the delay line. . . ”

Applicant submits that Iwamoto et al. do not disclose the limitations of Applicant's claims 1, 8, 10, 11, 18, 23, 27, 33, 34, 41, 45, 49, and 53. For these reasons, Applicant believes that the rejection of claims 1, 8, 10, 11, 18, 23, 27, 33, 34, 41, 45, 49, and 53 based on Iwamoto et al. has been overcome, and Applicant respectfully requests that the rejection be reconsidered and withdrawn.

Rejection of claims 1 and 9:

Claims 1 and 9 were rejected under 35 USC § 102(b) as being anticipated by Harlos et al. (U.S. Patent No. 4,805,021). Applicant has amended claim 1 from which claim 9 depends, and respectfully traverses the rejection.

Harlos et al. disclose a control circuit for calibrating a delay line (Figure 2), which includes a change-over switch 23, which selectively switches between outputting a luminance signal 24 or a delayed, amplified version 25 of the output 22 of switch 23. (See Figure 2, and col. 4, lines 24-37).

Applicant's claims 1 and 9 include at least the following features, which distinguish Applicant's claims from that which is disclosed by Harlos et al.:

“ . . . a signal selector circuit to switch between providing an external clock signal or a feedback clock signal as an input clock signal to a delay line based on a detected jitter between the external clock signal and the feedback clock signal . . . ”

Applicant respectfully submits that Harlos et al. do not disclose the limitations of Applicant's claims 1 and 9. For these reasons, Applicant believes that the rejection of claims 1

and 9 based on Harlos et al. has been overcome, and Applicant respectfully requests that the rejection be reconsidered and withdrawn.

Allowable Subject Matter

Claims 2-7, 11-17, 19-22, 28-32, 35-37, 42-44, 46-48, 50-52, and 54-56 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has amended claims 2, 5, 11, 19, 28, 35, 42, 46, 50, and 54 to include all of the limitations of their respective base claims (no claims were intervening). Accordingly, Applicant believes that claims 2, 5, 11, 19, 28, 35, 42, 46, 50, and 54 are in a condition for allowance, and respectfully requests that they be allowed.

With respect to claims 3-6, 7, 12-17, 20-22, 29-31, 36-37, 43-44, 47-48, 51-52, and 55-56, Applicant has amended claims 1, 10, 18, 27, 34, 41, 45, 49, and 53, respectively, from which these claims depend. Applicant believes that the base claims are allowable, and that, therefore, their dependent claims also are allowable. If the base claims are not held to be allowable in a future Office Action, Applicant may amend some or all of claims 3-6, 7, 12-17, 20-22, 29-31, 36-37, 43-44, 47-48, 51-52, and 55-56 to include the limitations of their respective base and intervening claims, if any.

Applicant acknowledges the allowance of claims 24-26, 38-40, and 57-59.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Sherry W. Schumm, at (480) 538-1735 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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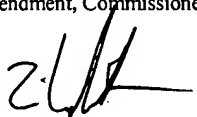
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3 day of February, 2005.

Tina Kohut

Name



Signature